

CBCS SCHEME

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18EE46

Fourth Semester B.E. Degree Examination, Jan./Feb. 2023 Operational Amplifiers and Linear ICs

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Explain the general stages of op-amp with a neat block diagram. (08 Marks)
 - Define explain the following terms:
 - Input Bias current
 - Input offset current.
 - CMRR. (06 Marks)
 - Explain with a neat circuit, scaling and averaging amplifier using op-amp in inverting configuration. (06 Marks)

OR

- Explain with a neat circuit diagram, instrumentation amplifier. (08 Marks)
 - For the circuit shown in Fig.Q2(b), determine the voltage V_1 at the non-inverting terminal and the output voltage V_0 . Assume that the op-amp is initially nulled.

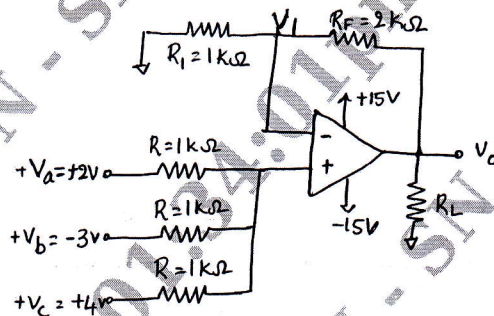


Fig. Q2(b)

- What are the characteristics of an ideal op-amp? Also explain voltage transfer characteristics curve of an op-amp. (06 Marks)

Module-2

- With a neat circuit diagram, explain working of an second order low pass filter and draw its typical frequency response curve. (10 Marks)
 - Explain working and design of voltages follower regulator. (06 Marks)
 - Explain the following terms with respect to voltage regulator.
 - Line regulation
 - Load regulation. (04 Marks)

OR

- Sketch the circuit of a series regulator that uses an IC op-amp as an error amplifier. Explain the circuit operation. Write equation for V_0 terms of V_Z . (10 Marks)
 - A DC power supply drops from 15V to 14.95V when the AC supply voltage falls by 10%. The output also falls from 15 to 14.9V. When the load current increases from zero to maximum. Calculate the source effect, load effect, line regulation and load regulation. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-3

- 5 a. Draw the circuit diagram of a triangular/rectangular waveform generator using op-amps. Sketch the circuit waveforms, and explain its circuit operation. (10 Marks)
- b. Draw the circuit diagram of an op-amp RC phase shift Oscillator. Sketch the circuit waveforms, and briefly explain the oscillator operation. (10 Marks)

OR

- 6 a. Using a 741 op-amp, calculate resistor values for the inverting Schmitt trigger circuit to give triggering points of $\pm 2V$. (04 Marks)
- b. With a neat diagram, explain :
i) Comparator as zero crossing detector (08 Marks)
ii) Voltage to current converter with grounded load. (08 Marks)
- c. With a neat diagram, explain the non-inverting Schmitt trigger circuit. (08 Marks)

Module-4

- 7 a. With a neat circuit diagram, explain the operation of precision full wave rectifier as a combination of half wave rectifier and a summing circuit. Also sketch the waveforms. (08 Marks)
- b. Explain the working principle of linear R_{amp} analog to digital converter. (06 Marks)
- c. Design a non-saturating precision half-wave rectifier to produce a 2V peak output from a 1MHz sine wave input with a 0.5V peak value. Use a Bipolar op-amp with a supply voltage of $\pm 15V$. (06 Marks)

OR

- 8 a. Explain R – 2R ladder digital to analog converter circuit. (10 Marks)
- b. A linear ramp ADC uses a 10-bit counter and a 15KHz clock frequency. The counter output is to be 111111111 when the input voltage is 100mV. Calculate the required ramp rate of change and the ADC conversion. (04 Marks)
- c. Explain working ADC using successive approximation method. (06 Marks)

Module-5

- 9 a. Draw the basic block diagram and waveforms for a PLL system. Identify each component part and explain its function. (10 Marks)
- b. With a neat diagram, explain the internal architecture of IC 555 timer. (10 Marks)

OR

- 10 a. Explain how XOR Gates can be used as phase detector in PLL. (08 Marks)
- b. Explain Monostable Multivibrator, realized using IC 555 timer. (08 Marks)
- c. Define the terms related to PLL.
i) Tracking range
ii) Capture range. (04 Marks)
